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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 6,768,163	)	Serial No. 09/961,355
	)	
Inventor(s): Tomoharu TANAKA *et al*	)	Filed: September 25, 2001
	)	
Issue Date: July 27, 2004	)	Attorney Docket No. 001701.00119

For: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND NONVOLATILE SEMICONDUCTOR MEMORY SYSTEM

REQUEST FOR CERTIFICATE OF CORRECTION

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building, Mail Stop: Certificate of Correction Branch
401 Dulany Street
Alexandria, VA 22314

Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322, this is a request for the issuance of a Certificate of Correction in the above-identified patent. Two (2) copies of PTO Form 1050 are appended. The complete Certificate of Correction involves one page.

The mistakes identified in the appended Form occurred through no fault of the Applicants, as clearly disclosed by the records of the application, which matured into this patent. Enclosed for your convenience are the relevant portions of the Amendment filed July 24, 2003.

Issuance of the Certificate of Correction containing the corrections is respectfully requested. Since these changes are necessitated through no fault of the Applicants, no fee is believed to be associated with this request. Nonetheless, should the Patent and Trademark Office determine that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: April 5, 2005

By: _____
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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 6,768,163

DATED: July 27, 2004

INVENTOR(S): Tomoharu TANAKA *et al*

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 12, Claim 1, Line 52:
Please replace "in which," with --in which--

In Column 13, Claim 2, Line 2:
Please replace "substrate stacked" with --substrate is stacked--

In Column 13, Claim 3, Line 6:
Please replace "substrate stacked" with --substrate is stacked--

In Column 14, Claim 18, Line 59:
Please replace ", in which," with --includes--

In Column 14, Claim 18, Line 60;
Please replace "defected" with --defective--

In Column 14, Claim 19, Line 64:
Please replace "in which," with --in which--

In Column 15, Claim 19, Line 1:
Please replace "in which," with --in which--

In Column 15, Claim 19, Line 9:
Please replace "capable is of" with --is capable of being--

In Column 15, Claim 20, Line 12;
Please replace "substrate stacked" with --substrate is stacked--

In Column 16, Claim 23, Line 11:
Please replace "package stacked" with --package is stacked--

In Column 16, Claim 24, Line 15:
Please replace "package stacked" with --package is stacked--

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U.S. PAT. NO 6,768,163

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@ $0.50 per page

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■ PATENT ☐ DESIGN B&W Ref. 001701-00119 Date 7/24/03
☐ HAND CARRY Group/Section _____ Bldg _____ Rm _____
Serial/Patent No. 09/910,865 Atty/Sec JMP:JNB:smn
Inventor Tomoharu TANAKA et al. Client Suzuye
Title NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND NONVOLATILE SEMICONDUCTOR MEMORY SYSTEM

The following has been received in the U.S. Patent and Trademark Office on the date stamped hereon:

☐ ____ total pp Spec., including: # of Claims ____ (# of independent claims ____): ☐ Abstract
☐ Drawings: ☐ Formal ☐ Informal # of distinct sheets ____: Figs. ____
☐ Declaration/Power of Attorney: ☐ Executed ☐ Unexecuted
☐ Assignment w/PTO Cover Sheet
☐ IDS w/PTO 1449 ☐ References ☐ w/Fee
☐ Preliminary Amendment
☐ Priority Claim (Foreign or U.S. Provisional. B&W # ____)
Country Appl. # Date
☐ w/Foreign Priority Document(s)
☐ Application: ☐ CIP ☐ Continuation ☐ Divisional
Parent Ser. No. ____ B&W# ____
☐ U.S. Provisional ____ pp Spec/Claims; Cover Sheet
☐ Response to Missing Parts/Requirements dtd ____
☐ Response to Notice to File Corrected Appln. Papers dtd ____
☐ Request for Expedited Foreign Filing License
☐ Request for Corrected: ☐ Filing Receipt ☐ Assignment
☐ Response to Restriction/Election Requirement

☐ Sequence Listing: ☐ Diskette ☐ Paper
■ Amendment ☐ Response: OA dtd 4-25-03
☐ Petition for Extension of Time until ____
☐ CPA ☐ RCE ☐ w/Ext of Time: OA dtd ____
☐ Request for Approval of Drawing Changes
☐ Notice of Appeal & Fee
☐ Brief: ☐ Appeal & Fee ☐ Reply
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☐ Amendment under 37 CFR 1.312
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B&W Rev. 5/01

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)
	)
Tomoharu TANAKA et al.	) Group Art Unit: 2811
	)
Serial No.: 09/961,355	) Examiner: Douglas W. Owens
	)
Filed: September 5, 2001	) Atty Dckt No.: 001701.00119
	)
For: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND NONVOLATILE SEMICONDUCTOR MEMORY SYSTEM	)

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This paper is responsive to the non-final Office Action mailed April 25, 2003 (paper no. 4). Applicants respectfully request that the above-identified application be amended as set forth herein, and that this application be reconsidered and allowed based on the following remarks.

IN THE CLAIMS

Please amend claims 1-3, 5, 6, 9-12, 15-29 as follows (all pending claims are reproduced for the Examiner's convenience):

1. (Currently Amended) A semiconductor integrated circuit device comprising:

a first semiconductor substrate, in which[[,]] a memory cell array including a plurality of nonvolatile semiconductor memory cells, a plurality of bit lines electrically connected to the memory cell array, a plurality of word lines electrically connected to the memory cell array, a plurality of input terminals, and a plurality of transfer gate transistors each having one end electrically connected to a corresponding one of the word lines and another end electrically connected to a corresponding ~~to~~ one of the input terminals, are provided; and

a second semiconductor substrate, in which, a plurality of output terminals electrically connected to the input terminals of the first semiconductor substrate, and a word line control circuit configured to control the word lines and electrically connected to the output terminals, are provided.

2. (Currently Amended) The device according to claim 1, wherein the second semiconductor substrate is stacked on the first semiconductor substrate.

3. (Currently Amended) The device according to claim 1, further comprising:

a plurality of first semiconductor substrates, wherein the second semiconductor substrate is stacked on at least one of the plurality of first semiconductor substrates.

4. (Original) The device according to claim 1, further comprising:

a first package which seals the first semiconductor substrate, the first package having a plurality of first terminals electrically connected to the input terminals of the first semiconductor substrate, the first terminals being provided on a side surface of the first package;

a second package which seals the second semiconductor substrate, the second package having a plurality of second terminals electrically connected to the output terminals of the second semiconductor substrate, the second terminals beings provided on a side surface of the second package; and

a plurality of wirings which electrically connects the first terminals of the first package

word lines and another end electrically connected to a corresponding ~~to~~ one of the input terminals, and a second shift register configured to control the transfer gate transistors, are provided; and

a second semiconductor substrate, in which[[,]] a plurality of output terminals electrically connected to the input terminals of the first semiconductor substrate, and a word line control circuit configured to control the word lines and electrically connected to the output terminals, are provided.

16. (Currently Amended) The device according to claim 15, wherein the second semiconductor substrate is stacked on the first semiconductor substrate.

17. (Currently Amended) The device according to claim 15, further comprising:

a plurality of first semiconductor substrates, wherein the second semiconductor substrate is stacked on at least one of the plurality of first semiconductor substrates.

18. (Currently Amended) The device according to claim 15, wherein the second semiconductor substrate[[,]] ~~in which,~~ includes a storage circuit which stores an address of a ~~defected~~ defective memory cell in the memory cell array[[,]] ~~is provided~~.

19. (Currently Amended) A nonvolatile semiconductor memory ~~system~~ package comprising:

a memory having a memory cell array including a plurality of nonvolatile semiconductor memory cells;

a control portion configured to control the memory;

a network interface connectable to a network;

a file management portion connected to the network interface configured to ~~manages~~ manage a ~~relation~~ relationship between a data file given from the network and an address of the memory cell array; and

a memory interface connected to the file management portion configured to convert a signal given from the network to a signal which is capable of being used at the control portion.

20. (Currently Amended) The ~~system~~ package according to claim 19, wherein the network interface corresponds to a transmission control protocol/internet protocol.

21. (Currently Amended) The ~~system~~ package according to claim 20, wherein the network interface is connectable to the network by using a file transfer protocol.

22. (Currently Amended) The ~~system~~ package according to claim 20, wherein the network interface is connectable to the network by using an anonymous file transfer protocol.

23. (Currently Amended) The ~~system~~ package according to claim 20, wherein the network interface is connectable to the network by using a point-to-point protocol.

24. (Currently Amended) A nonvolatile semiconductor memory device comprising:

a first semiconductor substrate, in which[[,]] a memory having a memory cell array including a plurality of nonvolatile semiconductor memory cells, is provided; and

a second semiconductor substrate, in which[[,]] a control portion configured to control the memory, a network interface connectable to a network, a file management portion connected to the network interface configured to ~~manages~~ manage a relation between a data file given from the network and an address of the memory cell array, and a memory interface connected to the file management portion configured to convert a signal given from the network to a signal which is capable of being used at the control portion, are provided.

25. (Currently Amended) The device according to claim 24, wherein the second semiconductor substrate is stacked on the first semiconductor substrate.

26. (Currently Amended) The device according to claim 24, further comprising:

a plurality of first semiconductor substrates, wherein the second semiconductor substrate is stacked on at least one of the plurality of first semiconductor substrates.

27. (Currently Amended) The device according to claim 24, further comprising:

a first package which seals the first semiconductor substrate, the first package having a plurality of first terminals electrically connected to the memory cell array, the first terminals being provided on a side surface of the first package; and

a second package which seals the second semiconductor substrate, the second package having a plurality of second terminals electrically connected to the memory interface, and a plurality of third terminals electrically connected to the network interface, the second terminals being provided on a side surface of the second package and the third terminals being provided on

a surface of the second package opposite to a lamination surface ~~with~~ of the first package;

a plurality of wirings which electrically connects the first terminals of the first package and the second terminals of the second package, the wirings being provided on the side surfaces of the first package and the second package.

28. (Currently Amended) The device according to claim 27, wherein the second package is stacked on a surface different from the side surface of the first package.

29. (Currently Amended) The device according to claim 27, further comprising:

a plurality of first packages,

wherein the second package is stacked on a surface different from the side surface of at least one of the first packages.

30. (Original) The device according to claim 27, further comprising:

a third package which seals the first package, the second package and the wiring, the third package having a plurality of fourth terminals electrically connected to the third terminals of the second package.

31. (Original) The device according to claim 29, further comprising:

a third package which seals the first packages, the second package and the wirings, the third package having a plurality of fourth terminals electrically connected to the third terminals of the second package.

Please add claims 32 and 33 as follows:

32. (New) The package according to claim 19, wherein the package works as a storage device for the equipment.

33. (New) The package according to claim 19, wherein the package is also connectable to equipment disconnected from the network.